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HMC7043 Data Sheet Changes

Rev D

Data Sheet Changes

REV B: OLD SPECIFICATIONS

- Specifications Table 4, Page 5.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK INPUT (CLKIN) CHARACTERISTICS					
Recommended Input Power, AC-Coupled					
Differential	−6		+8	dBm	
Single-Ended[1]	−10		+6	dBm	Noise floor degrade by 3 dB at f_{CLKIN} = 2400 MHz
Return Loss		−12		dB	When terminated with 100 Ω differential
Clock Input Frequency (f_{CLKIN})	200		3200	MHz	Fundamental mode; if <1 GHz, set the low frequency clock input path enable bit (Register 0x0064, Bit 0)
	200		6000	MHz	Using clock input ÷ 2

REV D: NEW SPECIFICATIONS

- Specifications Table 4, Page 5 and 6.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (CLKIN)					
Recommended Input Power, AC-Coupled					
Differential	−6		+8	dBm	
Single-Ended[1]	−10		+6	dBm	Noise floor degrade by 3 dB at f_{CLKIN} = 2400 MHz
Return Loss		−12		dB	When terminated with 100 Ω differential
Clock Input Frequency (f_{CLKIN})	200			MHz	When all channel dividers are equal to one or channels are in the fundamental mode. If <1 GHz, set the low frequency external VCO path bit (Register 0x0064, Bit 0)
	450			MHz	When channel dividers are larger than 1 and synchronization is needed
			3200	MHz	Clock Input Divider is disabled. Register 0x0064[1] = 0
			6000	MHz	Clock Input Divider is enabled. Register 0x0064[1] = 1

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